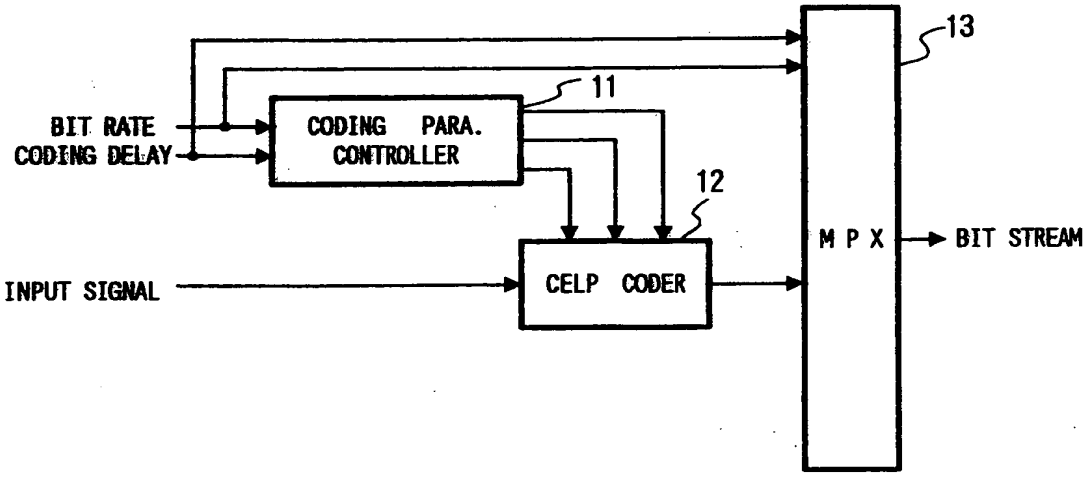
FIG. 1


13
11
BIT RATE
CODING DELAY
CODING PARA. CONTROLLER
12
M P X
BIT STREAM
INPUT SIGNAL
CELP CODER

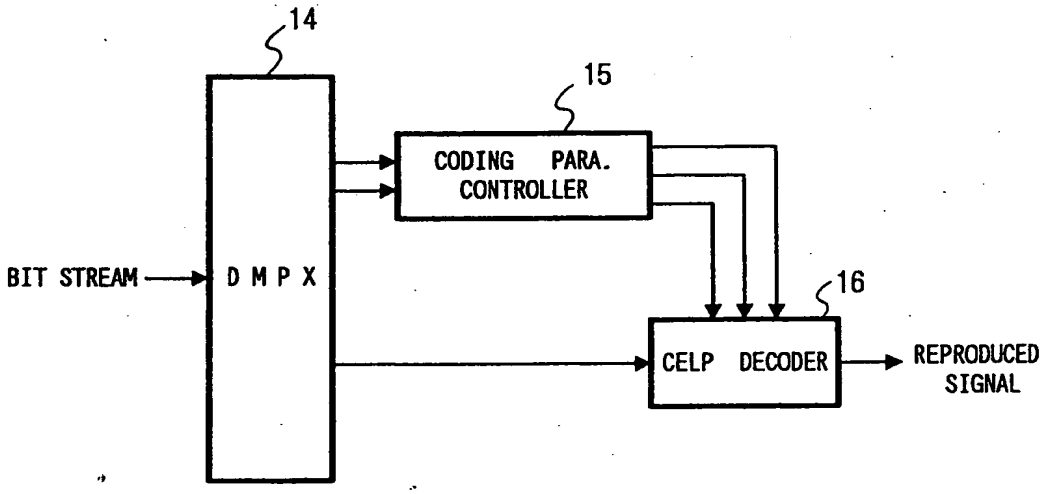

14
15
CODING PARA. CONTROLLER
BIT STREAM
D M P X
16
CELP DECODER
REPRODUCED SIGNAL

FIG. 2

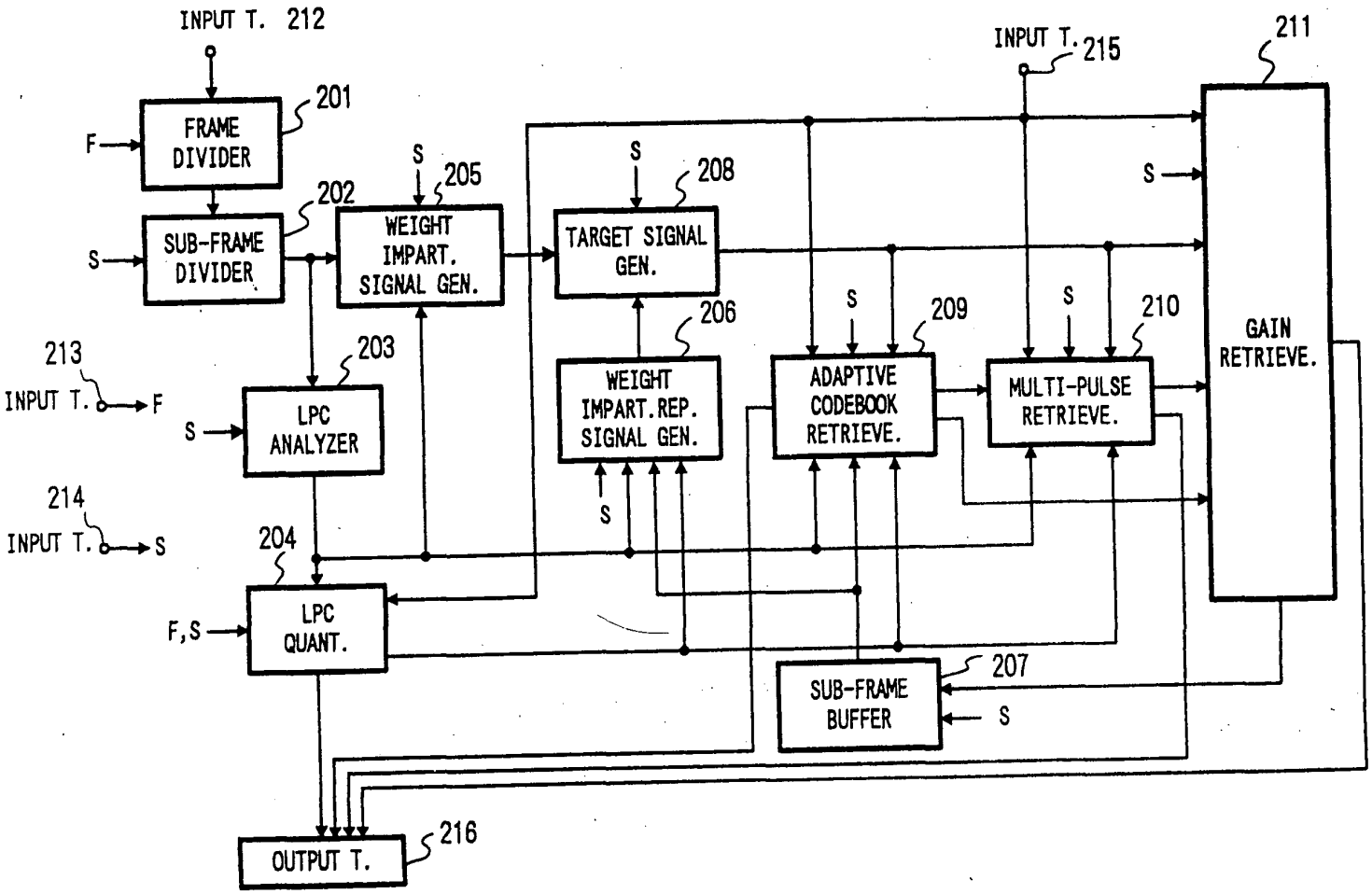

INPUT T. 212
201
FRAME DIVIDER
F
202
SUB-FRAME DIVIDER
S
205
S
WEIGHT IMPART. SIGNAL GEN.
208
S
TARGET SIGNAL GEN.
INPUT T. 215
211
S
GAIN RETRIEVE.
213
INPUT T.
F
203
S
LPC ANALYZER
206
WEIGHT IMPART. REP. SIGNAL GEN.
S
209
S
ADAPTIVE CODEBOOK RETRIEVE.
210
S
MULTI-PULSE RETRIEVE.
214
INPUT T.
S
204
F,S
LPC QUANT.
207
SUB-FRAME BUFFER
S
216
OUTPUT T.

FIG. 3

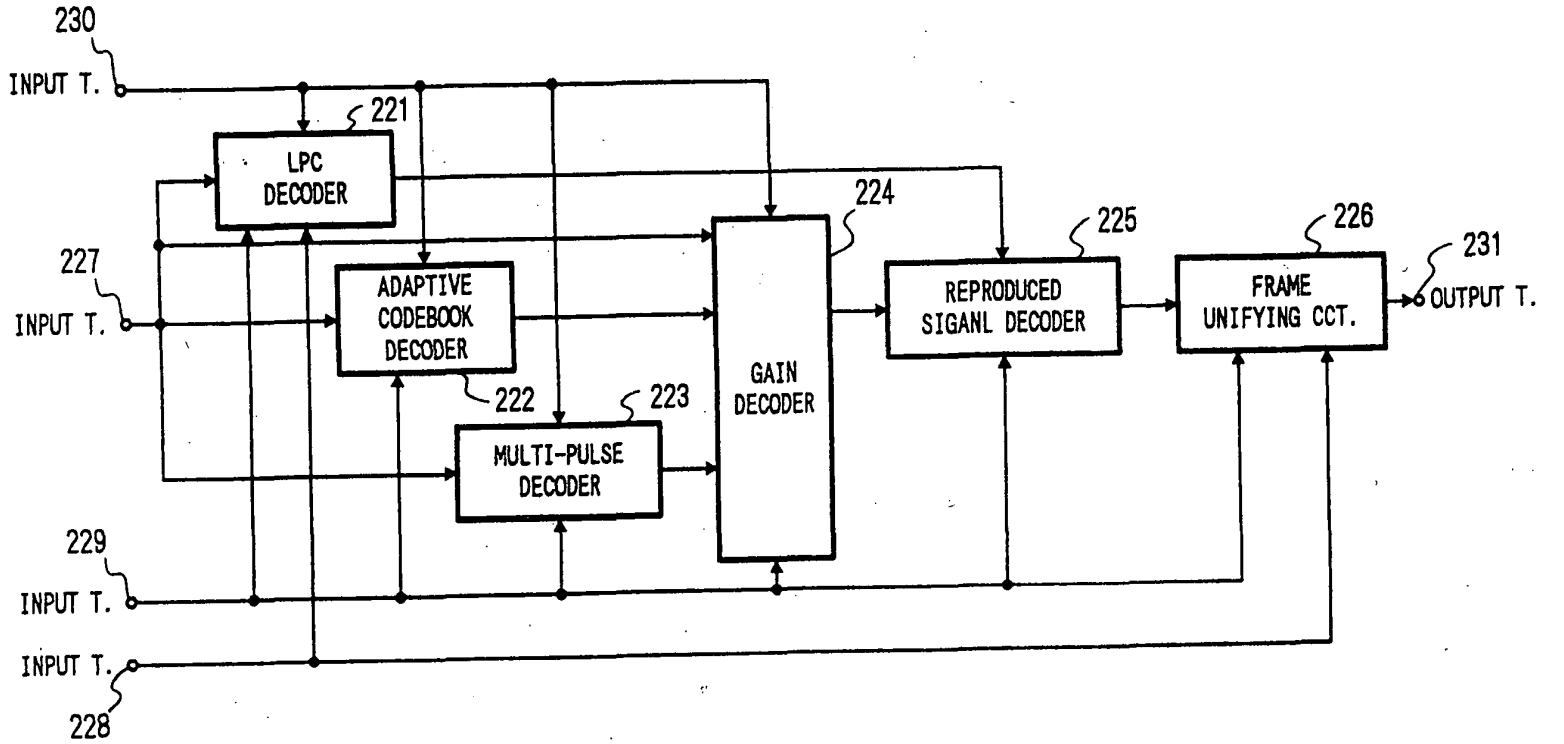
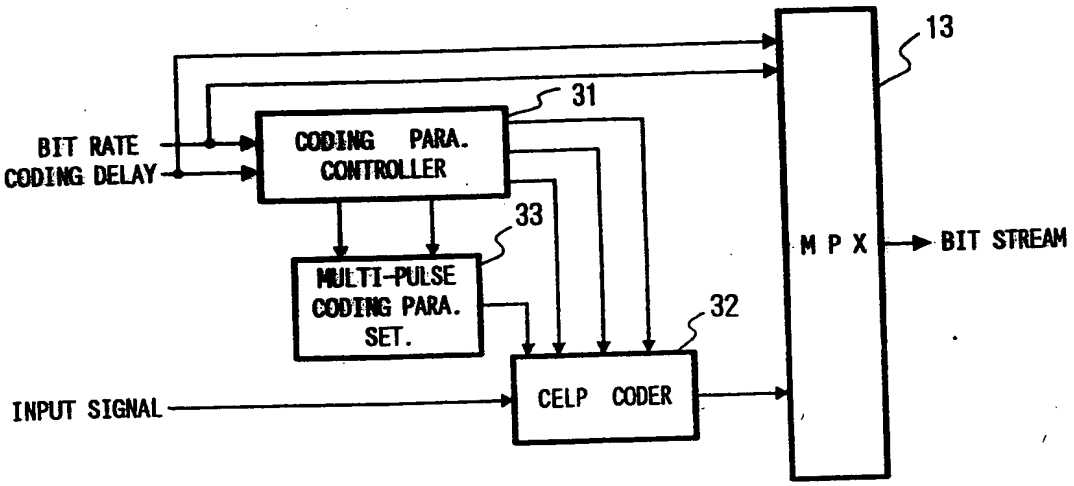

230
INPUT T.
221
LPC DECODER
227
INPUT T.
ADAPTIVE CODEBOOK DECODER
222
223
MULTI-PULSE DECODER
224
GAIN DECODER
225
REPRODUCED SIGANL DECODER
226
FRAME UNIFYING CCT.
231
OUTPUT T.
229
INPUT T.
INPUT T.
228

FIG. 4


13
31
BIT RATE
CODING DELAY
CODING PARA. CONTROLLER
33
MULTI-PULSE CODING PARA. SET.
32
M P X
BIT STREAM
INPUT SIGNAL
CELP CODER

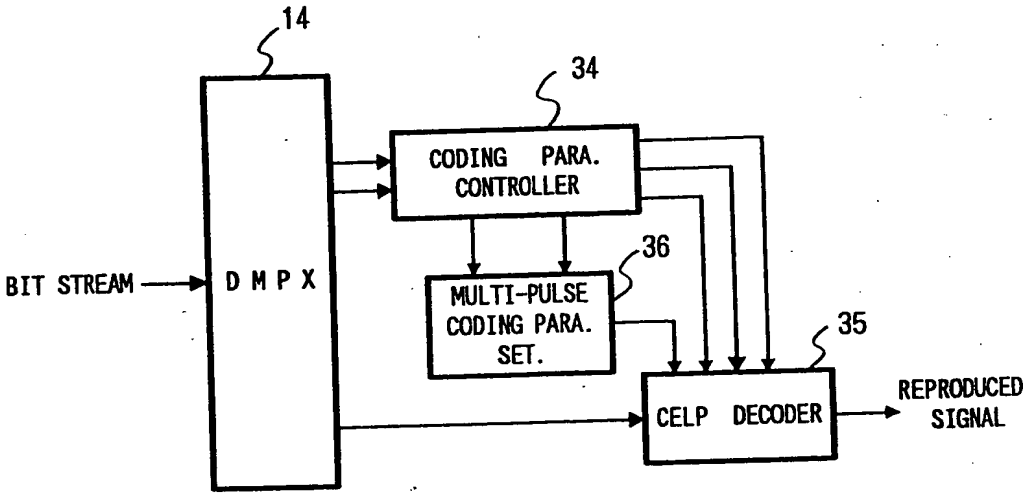

14
34
CODING PARA. CONTROLLER
BIT STREAM
D M P X
36
MULTI-PULSE CODING PARA. SET.
35
CELP DECODER
REPRODUCED SIGNAL

FIG.5

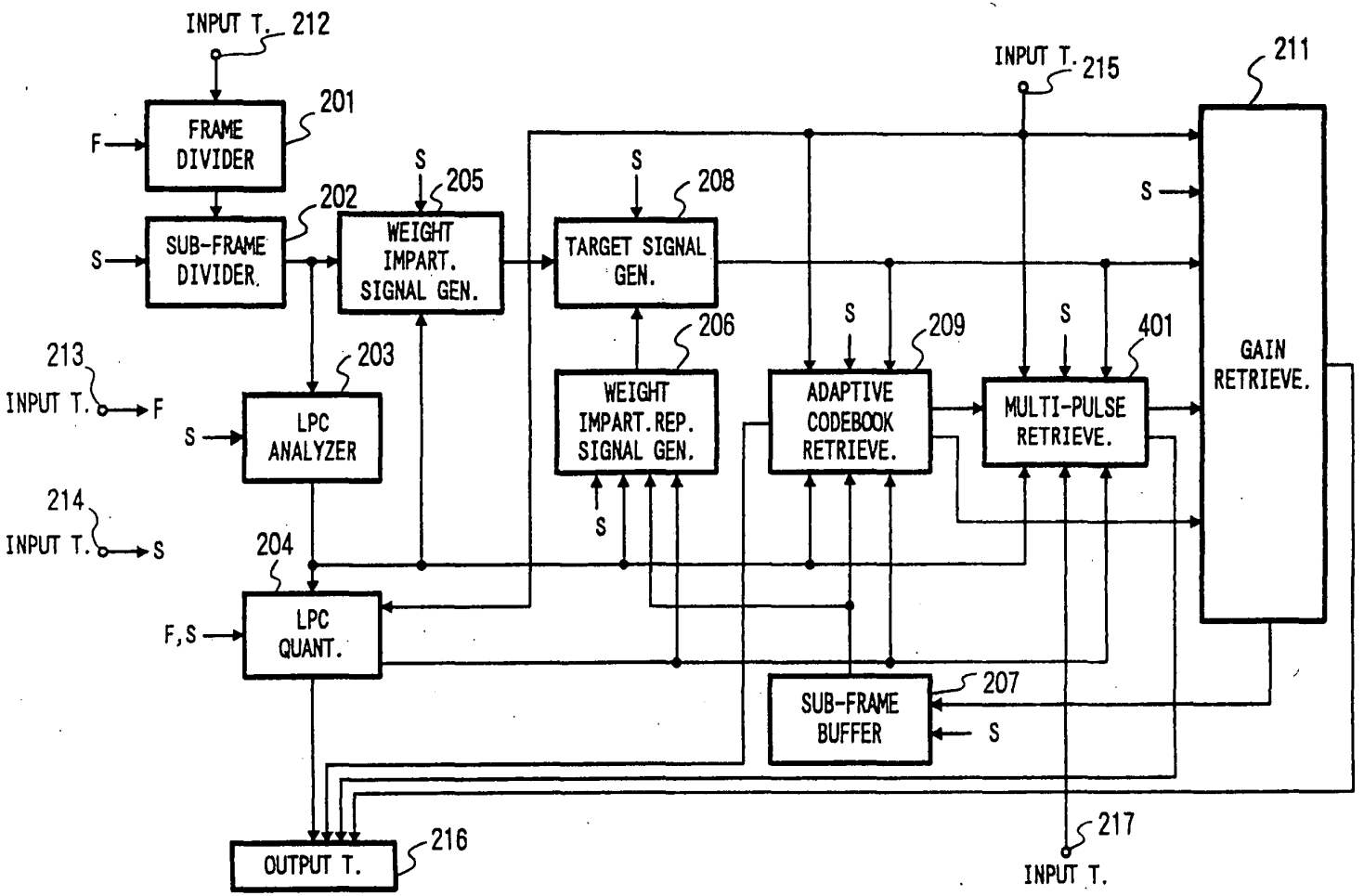

INPUT T.
212
FRAME DIVIDER
201
F
SUB-FRAME DIVIDER.
202
S
WEIGHT IMPART. SIGNAL GEN.
205
S
TARGET SIGNAL GEN.
208
S
INPUT T.
215
211
GAIN RETRIEVE.
213
INPUT T.
F
LPC ANALYZER
203
S
214
INPUT T.
S
WEIGHT IMPART.REP. SIGNAL GEN.
206
S
ADAPTIVE CODEBOOK RETRIEVE.
209
S
MULTI-PULSE RETRIEVE.
401
204
LPC QUANT.
F,S
SUB-FRAME BUFFER
207
S
OUTPUT T.
216
217
INPUT T.

FIG. 6

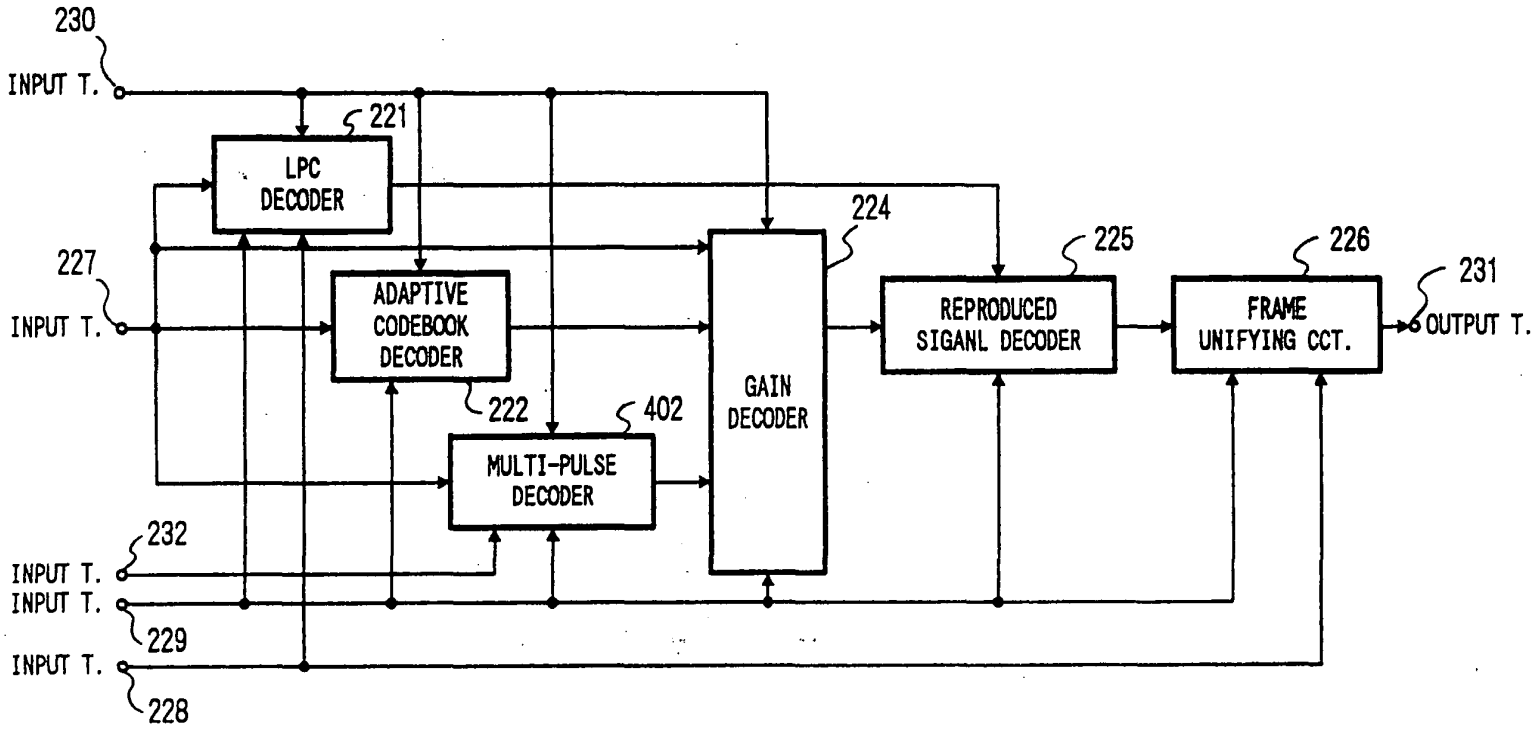

230
INPUT T.
221
LPC DECODER
227
INPUT T.
ADAPTIVE CODEBOOK DECODER
222
402
MULTI-PULSE DECODER
224
GAIN DECODER
225
REPRODUCED SIGANL DECODER
226
FRAME UNIFYING CCT.
231
OUTPUT T.
232
INPUT T.
INPUT T.
229
INPUT T.
228

FIG. 7

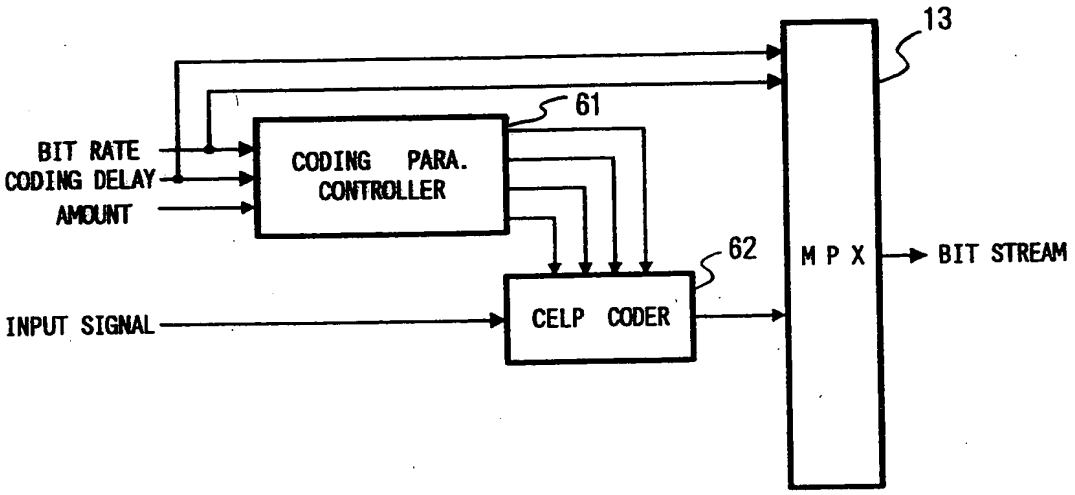

13
61
BIT RATE
CODING DELAY
AMOUNT
CODING PARA. CONTROLLER
62
M P X
BIT STREAM
INPUT SIGNAL
CELP CODER

FIG. 8

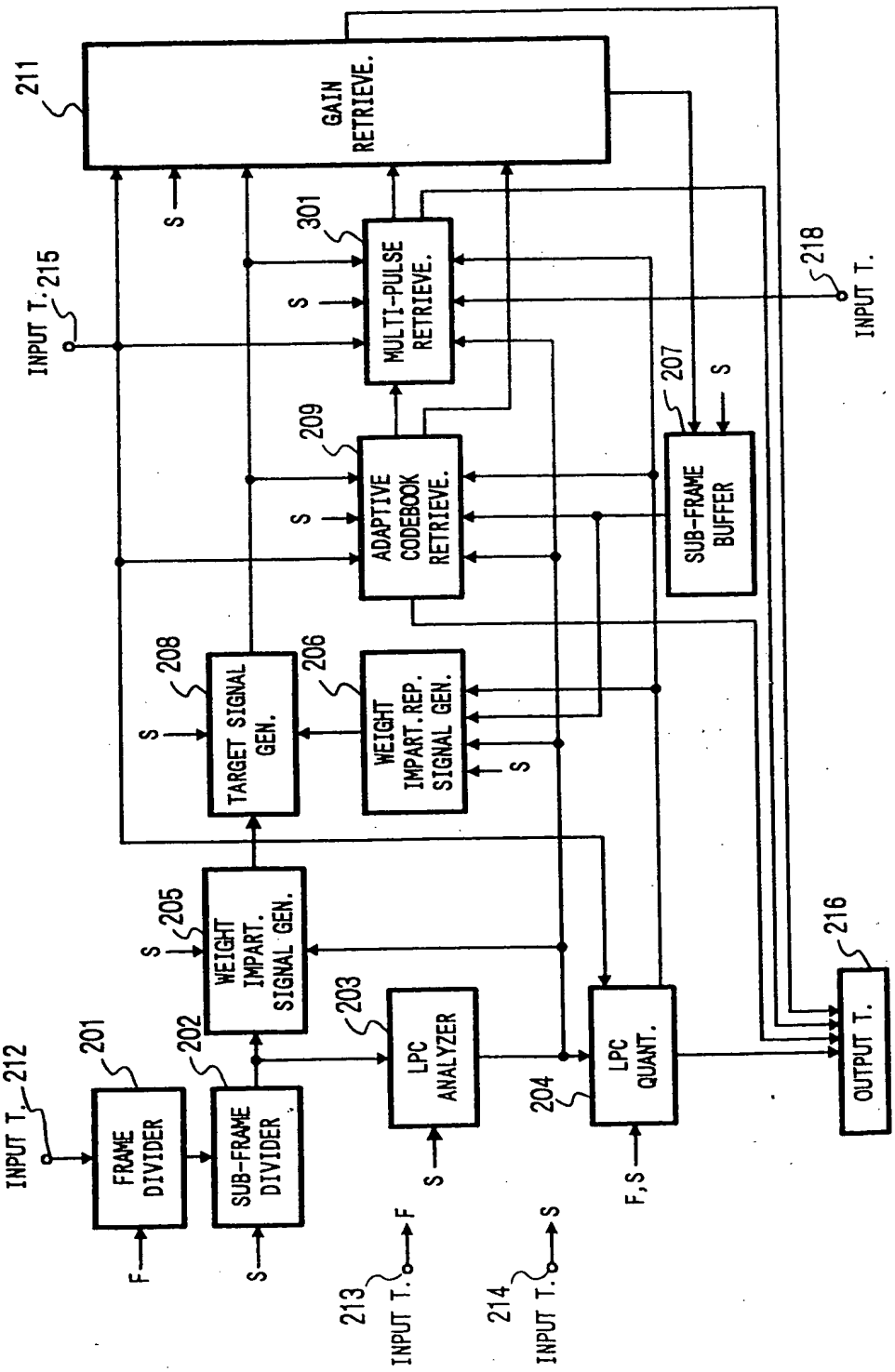

INPUT T.
212
FRAME DIVIDER
201
SUB-FRAME DIVIDER
202
WEIGHT IMPART. SIGNAL GEN.
205
TARGET SIGNAL GEN.
208
WEIGHT IMPART. REP. SIGNAL GEN.
206
ADAPTIVE CODEBOOK RETRIEVE.
209
MULTI-PULSE RETRIEVE.
301
GAIN RETRIEVE.
211
LPC ANALYZER
203
LPC QUANT.
204
SUB-FRAME BUFFER
207
OUTPUT T.
216
INPUT T.
215
INPUT T.
218
INPUT T.
213
INPUT T.
214
F
S
S
S
S
S
S
S
S
S
F,S
F,S

FIG. 9

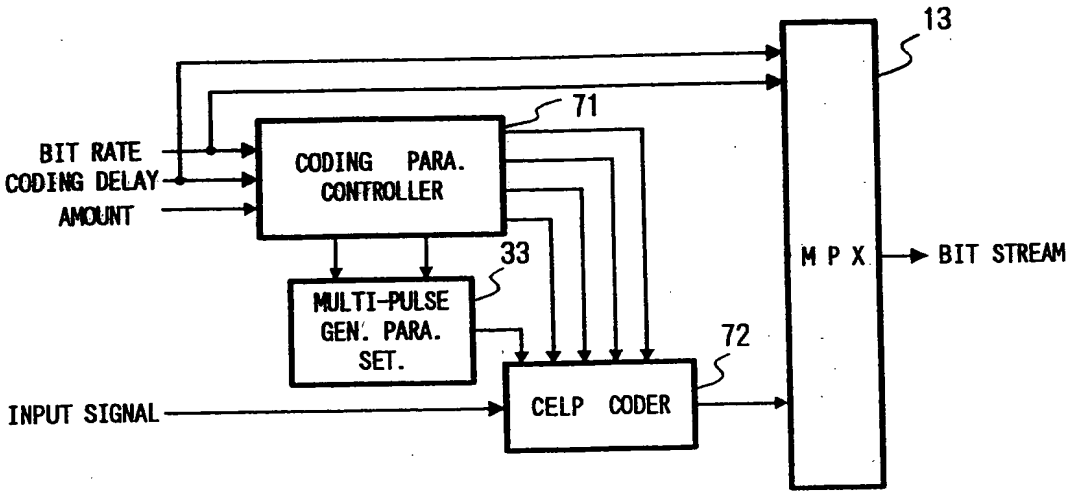

13
71
BIT RATE
CODING DELAY
AMOUNT
CODING PARA. CONTROLLER
33
MULTI-PULSE GEN. PARA. SET.
72
INPUT SIGNAL
CELP CODER
M P X
BIT STREAM

FIG. 10

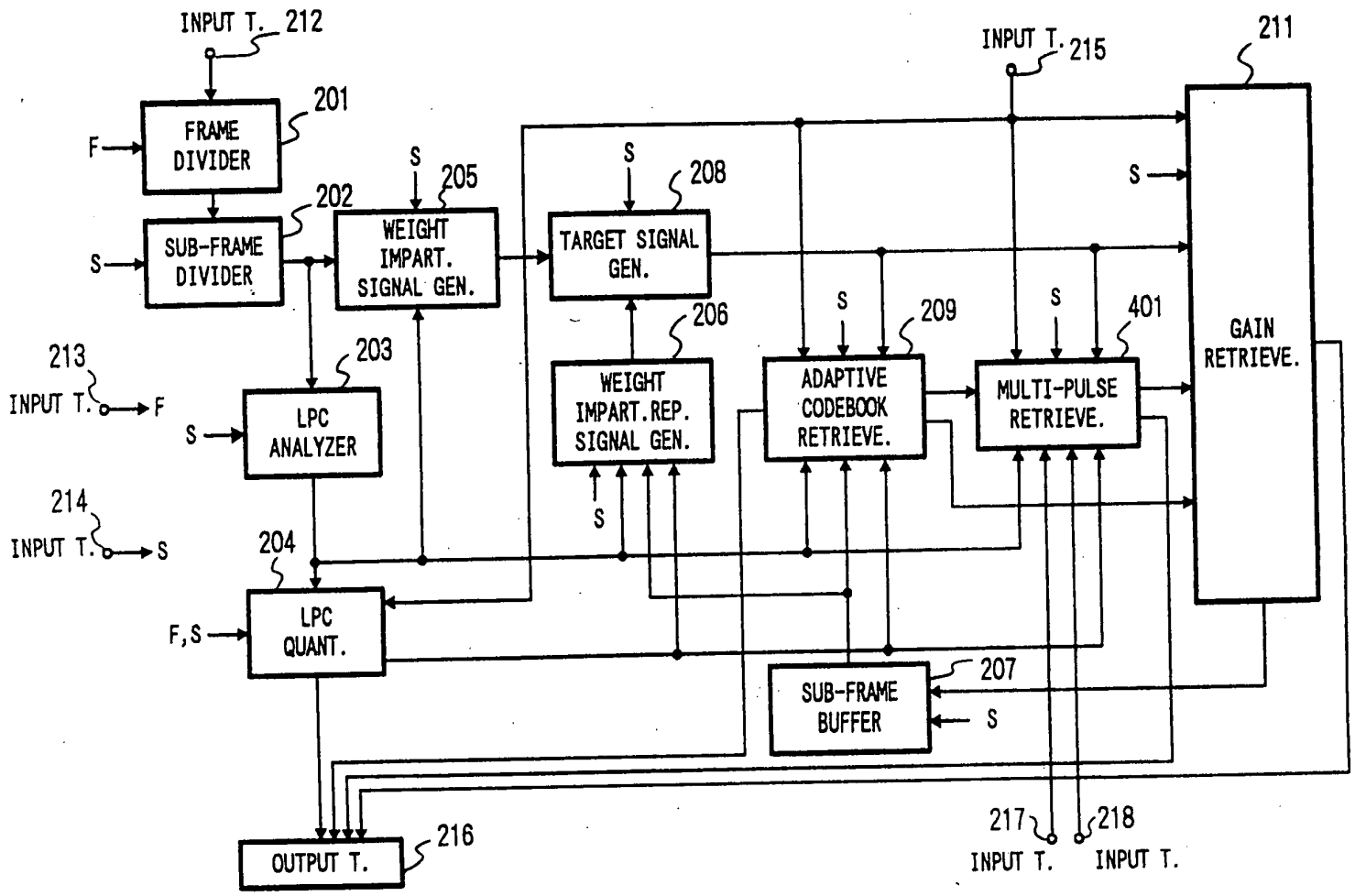
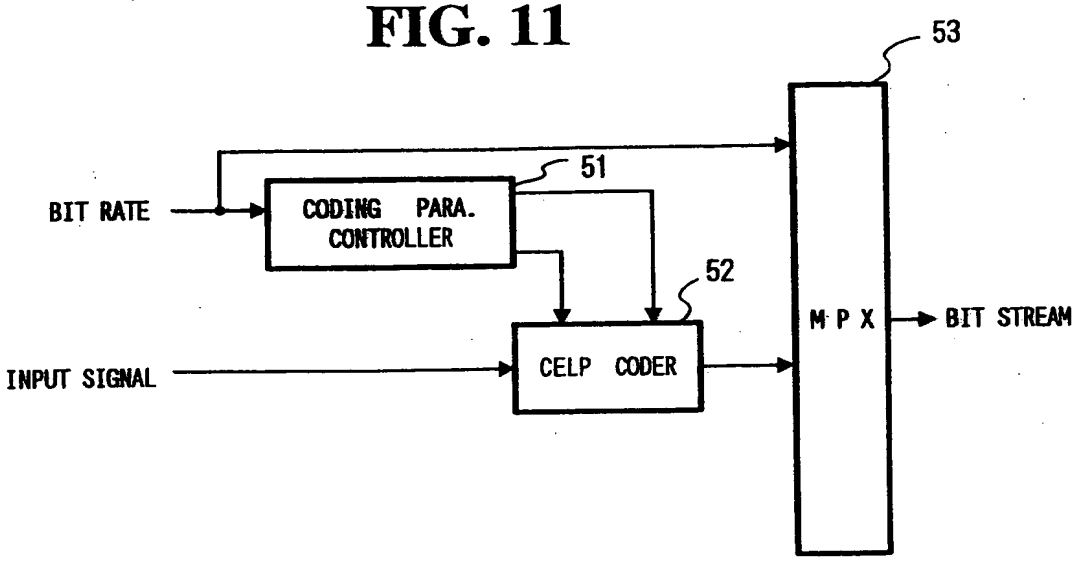
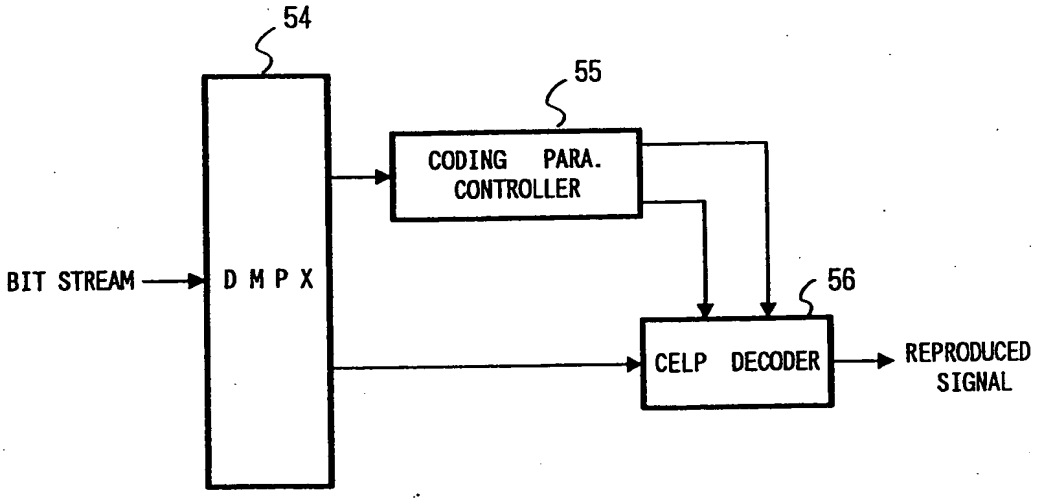

INPUT T.
212
201
FRAME DIVIDER
F
202
SUB-FRAME DIVIDER
S
205
WEIGHT IMPART. SIGNAL GEN.
208
TARGET SIGNAL GEN.
206
WEIGHT IMPART.REP. SIGNAL GEN.
209
ADAPTIVE CODEBOOK RETRIEVE.
401
MULTI-PULSE RETRIEVE.
211
GAIN RETRIEVE.
INPUT T.
215
213
INPUT T.
F
203
LPC ANALYZER
214
INPUT T.
S
204
LPC QUANT.
F,S
207
SUB-FRAME BUFFER
216
OUTPUT T.
217
INPUT T.
218
INPUT T.

FIG. 11


53
51
BIT RATE
CODING PARA. CONTROLLER
52
M P X
BIT STREAM
INPUT SIGNAL
CELP CODER


54
55
CODING PARA. CONTROLLER
BIT STREAM
D M P X
56
CELP DECODER
REPRODUCED SIGNAL